

CLAIMS

1. A clocked inverter circuit in which all transistors are same-channel transistors, the clocked inverter circuit comprising:

5 a first series circuit in which a set of transistors that switch operations in a complimentary manner based on clocks are connected in series, an input signal being input to one end of the series circuit;

10 a first inverter circuit including a set of transistors, a connection midpoint of the first series circuit being connected to a gate of one of the transistors; and a second inverter circuit including a set of transistors that input an output signal, whose signal level varies in response to an output of the connection midpoint.

15 of the first series circuit, to an opposite end of the first series circuit.

2. A latch circuit in which all transistors are same-channel transistors, the latch circuit comprising:

20 a first series circuit in which a set of transistors whose operations are switched in a complimentary manner based on clocks are connected in series, an input signal being input to one end of the series circuit;

25 a first inverter circuit including a set of transistors, a connection midpoint of the first series circuit being

connected to a gate of one of the transistors; and
a second inverter circuit including a set of
transistors that input an output signal, whose signal level
varies in response to an output of the connection midpoint
5 of the first series circuit, to an opposite end of the first
series circuit.

3. The latch circuit according to claim 2, wherein the
second inverter circuit is an inverter circuit that inputs
10 an output signal of the first inverter circuit to one of the
transistors.

4. The latch circuit according to claim 3, further having
a second system relative to a first system including the
15 first series circuit, the first inverter circuit, and the
second inverter circuit, the second system including a first
series circuit, a first inverter circuit, and a second
inverter circuit which correspond to the first series
circuit, the first inverter circuit, and the second inverter
20 circuit included in the first system;

wherein an inverse signal of the input signal is input
to one end of the first series circuit in the second system
and an output of the second inverter circuit in the second
system is input to an opposite end of the first series
25 circuit in the second system,

the connection midpoint of the first series circuit in the first system is connected to a gate of another one of the transistors in the first inverter circuit in the second system, and

5 an output of the first inverter circuit in the first system is input to a gate of another one of the transistors in the second inverter circuit in the second system; and

wherein a connection midpoint of the first series circuit in the second system is connected to a gate of 10 another one of the transistors in the first inverter circuit in the first system, and

an output of the first inverter circuit in the second system is input to a gate of another one of the transistors in the second inverter circuit in the first system.

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5. The latch circuit according to claim 2, further having a second series circuit including a set of transistors that switch operations in a complimentary manner in conjunction with the set of transistors of the first series circuit,

20 wherein, in the second series circuit, a reverse signal of the input signal is input to an end corresponding to the one end of the first series circuit and an output of the first inverter circuit is input to an end corresponding to the opposite end of the first series circuit;

25 whereina gate of another one of the transistors in the

first inverter circuit is connected to a connection midpoint of the set of transistors in the second series circuit; and wherein the connection midpoint of the second series circuit is connected to a gate of one of the transistors in

5 the second inverter circuit and a gate of another one of the transistors in the second inverter circuit is connected to the connection midpoint of the set of transistors in the first series circuit.

10 6. A shift register circuit in which a latch circuit sequentially transfers a drive signal, wherein, in the latch circuit, all transistors are formed by same-channel transistors, and the latch circuit comprises:

15 a first series circuit in which a set of transistors that switch operations in a complementary manner based on clocks are connected in series, an input signal being input to one end of the series circuit;

20 a first inverter circuit including a set of transistors, a connection midpoint of the first series circuit being connected to a gate of one of the transistors; and

25 a second inverter circuit including a set of transistors that input an output signal, whose signal level varies in response to an output of the connection midpoint of the first series circuit, to an opposite end of the first

series circuit.

7. A drive circuit for a display apparatus in which pixels are arranged in a matrix,

5 wherein a shift register circuit including latch circuits sequentially transfers drive signals to generate drive signals for the pixels, and

wherein, in the latch circuit, all transistors are formed by same-channel transistors, and the latch circuit
10 comprises:

a first series circuit in which a set of transistors that switch operations in a complementary manner based on clocks are connected in series, an input signal being input to one end of the series circuit;

15 a first inverter circuit including a set of transistors, a connection midpoint of the first series circuit being connected to a gate of one of the transistors; and

a second inverter circuit including a set of transistors that input an output signal, whose signal level
20 varies in response to an output of the connection midpoint of the first series circuit, to an opposite end of the first series circuit.

8. A display apparatus in which pixels are arranged in a
25 matrix,

wherein a shift register circuit including latch circuits sequentially transfers drive signals to generate drive signals for the pixels, and

5 wherein, in the latch circuit, all transistors are formed by same-channel transistors, and the latch circuit comprises:

a first series circuit in which a set of transistors that switch operations in a complementary manner based on clocks are connected in series, an input signal being input
10 to one end of the series circuit;

a first inverter circuit including a set of transistors, a connection midpoint of the first series circuit being connected to a gate of one of the transistors; and

15 a second inverter circuit including a set of transistors that input an output signal, whose signal level varies in response to an output of the connection midpoint of the first series circuit, to an opposite end of the first series circuit.